SEE characterization for a Quad 12-bit 1.6 GSps ADC, Digitizing up to 6.4 GSps

O. Bonnet, R. Pilard, S. Pelé, Teledyne e2v, Avenue de Rochepleine, 38521 Saint-Egrève Cedex, France

RADECS 2021
VIENNA, 13-17 September

Overview

The EV12AQ600 is a quad channel 12-bit 1.6GSps ADC, with a Cross-Point-Switch which allows multi-mode operation with the capability to interleave the four independent cores in order to reach higher sampling rates, up to 6.4GSps.

After a successfully Total Ionizing Dose test (with a low dose rate of 36Rad/h, and up to a total dose of 150krad), it was submitted to a heavy ions test, in order to evaluate its sensibility to Single Event Effect up to a LET of 67 MeV.cm²/mg. This test was performed at RADEF (University of Jyväskylä) in November 2020.

Product description, test method

A) Product Description

This device is a quad channel 12-bit 1.6GSps ADC, C-band capable, embedding a cross point switch for flexibility and allows multi-mode operation with the capability to interleave the four independent cores in order to reach higher sampling rates. In 4-channel operating mode, the four cores can sample, in phase, four independent inputs at 1.6 GSps. In 2-channel operating mode, the cores are interleaved by 2 in order to reach 3.2 GSps sampling rate on each of the two inputs. In 1-channel operating mode, a single input is propagated to each of the four cores which are interleaved by 4 in order to reach a sampling rate of 6.4 GSps. This high flexibility enables digitization of IF and RF signals with up to 3.2 GHz of instantaneous bandwidth.

Table 1: Single core, 4-Channel mode at 1.6GSps

Output Level	Fin (MHz)	ENOB (bit)	SNR (dB_{FS})	SFDR (dB_{FS})
-1 dB_{FS} (NFPBW)	100 (NZ1)	8.7/(9.6)*	54.6/(59.9)*	73.3
	780 (NZ1)	8.7/(9.5)*	54.3/(59.4)*	73.4
	1580 (NZ2)	8.4/(9.1)*	53.4/(58.4)*	64.3
	2380 (NZ3)	8.1/(8.8)*	51.3/(56.3)*	63.6
-8 dB_{FS} (EFPBW)	3180 (NZ4)	8.4/(9.2)*	52.5/(57.7)*	66.6
	3980 (NZ5)	8.3/(9.2)*	52.2/(57.3)*	70.6
	4780 (NZ6)	8.2/(8.9)*	51.7/(56.8)*	61.8
	5580 (NZ7)	8.1/(8.7)*	51.3/(56.3)*	67.1

(*) Averaged simultaneous sampling by averaging the samples of the 4 cores when they are in phase.

SFDR at -8 dBFS is better than 60 dBFS up to the 6th Nyquist zone and ENOB is better than 8.0 bit.

SFDR at -8 dBFS, without H2 and H3 harmonics, is better than 74 dBFS up to the 8th Nyquist zone.

Table 2: Interleaved cores, 1-channel mode at 6.4 GSps

Output level	Fin (MHz)	ENOB (bit)	SFDR (dB_{FS})
-1 dB_{FS}	100 (NZ1)	8.6	66.2
	2380 (NZ1)	8.0	64.7
-8 dB_{FS}	3980 (NZ2)	7.9	53.2

B) Test method

1) SEL test principle

Runs are performed up to a fluence of 1E+7.cm-² with only SEL monitoring.

Table.3 : SEL configuration

Mode	Channel Mode	Clock Frequency	Analog Input Frequency
1	1	6.4 Gsps	3.19950264GHz
2	2		
3	4		

The maximum supply voltage and a temperature of Tj=125°C are used for this test.

2) SET test principle

Runs are performed up to a fluence of 1E+6 cm-2 for the SET, SEU and SEFI detection.

The beat frequency method, which was successfully used on our previous data converters, was used to perform the dynamic test. The clock was set at the frequency of FClock=6.4GHz and the input received a frequency of Fin=3.19950264GHz. In this condition, the beat frequency at the outputs was 497.359 kHz.

3) SEU/SEFI test principle

A SEFI was considered if :

- Eight hundred successive conversions were out the tolerance band
- Successive conversions were identical
- 10 successive errors were observed on CLK, CB2 (timestamp) and CB1 (parity bit)

Three steps were performed to restart the DUT in normal functional when a SEFI was detected:

- SEFI 1: The registers were read, next a new synchronization of ADC is performed. In this case the SEFI was counted like a SEFI on serial communication (SEFI_COM).
- SEFI 2: If the SEFI was not defused, registers were read and a next reset was applied. Then, registers were written and a synchronization of the ADC was performed.
- SEFI 3: If the SEFI state was still observed, registers were read and a ON/OFF cycle on power supply was performed. A reset was then applied and registers were written with a synchronization of the ADC

SEE results

A) SEL results

No SEL was observed up to a LET of 67.0 MeV.cm²/mg, Xenon heavy ion.

B) SET on SSO results

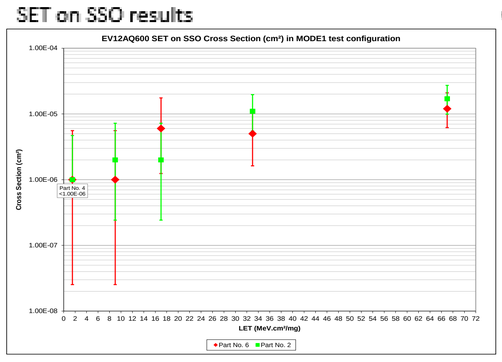

Fig.1: SET on SSO cross section curve in MODE1 test configuration

C) SET on SYNCO results

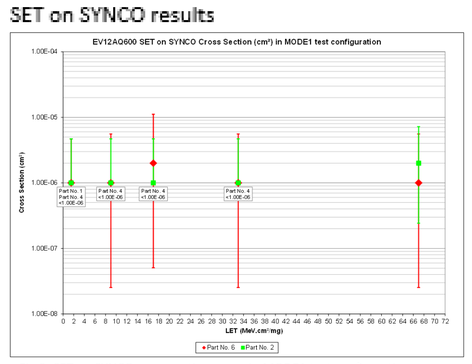

Fig.2: SET on SYNCO cross section curve in MODE1 test configuration

D) SEU results on core A, B, C and D

No LET threshold was found with available heavy ions during this test campaign

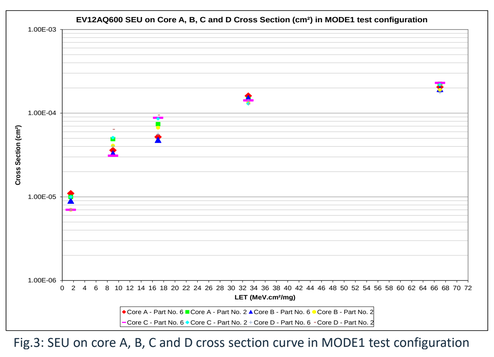

Fig.3: SEU on core A, B, C and D cross section curve in MODE1 test configuration

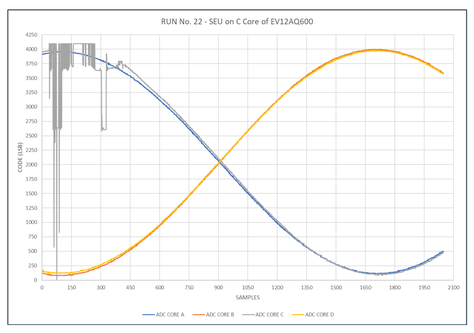

Fig.4: SEU example on C Core in MODE1 configuration

E) SEU on serial communication test results

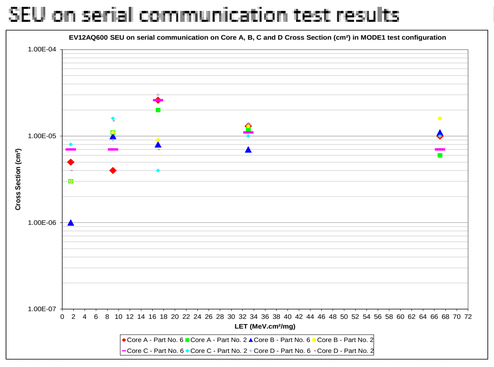

Fig.5: SEU on serial lanes of core A, B, C and D cross section curve in MODE1 configuration

F) SEFI on serial communication test results

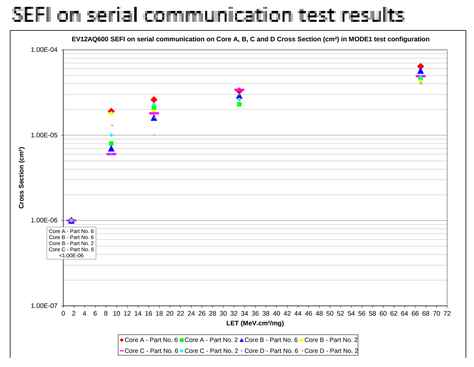

Fig.6: SEFI on serial lanes of core A, B, C and D cross section curve in MODE1 configuration

Each SEFI was easy to manage as:

- The SEFIs were easy to detect: Either the parity bit of the concern serial link was set to '1', either the CLK, CB2 and CB1 were erroneous during at least 10 clock cycles
- The SEFIs were easy to solve: A simple SYNC was enough to fully reset the device in the correct behavioral

As all the SEFI1 were solved by the SYNC command, no SEFI2 and SEFI3 were detected.

Conclusion

The EV12AQ600 Quad channel 12 bits 1.6GSps ADC from Teledyne-E2V has successfully passed this heavy ions test. The latch-up immunity up to a LET of 67 MeV.cm²/mg, the perfect similarity of the four cores and the very good performances of both, SSO and SYNCO signals must be particularly noted.

Those results complete the previous TID results and prove that this device is usable for most of the space applications like long-term missions or GEO satellites.

INTERSTELLAR

This project has received funding from the European Union™ Horizon 2020 research and innovation programme under grant agreement No 730165.

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